CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising a memory cell array in which memory cells respectively having one first electrode and a pair of second electrodes and capable of reading stored contents correspondingly to the potential of said first electrode in accordance with a state of the electrical connection between said second electrodes are arranged in the row and the column directions like a matrix, wherein

said memory cell array is constituted by connecting the first electrodes of said memory cells in the same row to a common word line, connecting said second electrodes each other between two of said memory cells adjacent to each other in the row direction, connecting one-hand said second electrodes in said memory cells in the same column to a common bit line, and connecting the other-hand said second electrodes in said memory cells in the same column to a common virtual ground line and moreover constituted by being divided into at least a plurality columns of subarrays,

memory cell columns at the both ends of said subarrays are constituted so that said second electrodes are not connected each other between two of said memory cells adjacent to each other in the row direction at the both sides of boundaries between said subarrays but they are separated from each other and respectively connected to an independent bit line or virtual ground line, and

one of said word lines, one of said bit lines, and one of said virtual ground lines are selected for each of said subarrays and one memory cell from which data will be read is selected.

2. A semiconductor memory device comprising a memory cell array in which memory cells respectively having one first electrode and a pair of second electrodes and capable of reading stored contents correspondingly to the potential of said first electrode in accordance with a state of the electrical connection between said second electrodes are arranged in the row and the column directions like a matrix, wherein

said memory cell array is constituted by connecting the first electrodes of said memory cells in the same row to a common word line, connecting said second electrodes each other between two of said memory cells adjacent in the row direction, connecting one-hand said second electrodes in said memory cells in the same column to a common bit line, and connecting the other-hand said second electrodes in said memory cells to a common virtual ground line and moreover constituted by being divided into at least a plurality columns of subarrays,

in the case of memory cell columns at the both ends of said subarrays, said second electrodes are not connected each other between two of said memory cells adjacent in the row direction at the both sides of boundaries between said subarrays but they are separated from each other and connected to independent bit lines or virtual ground lines, and

each of said bit lines and each of said virtual ground lines respectively have functions of the both and when one of them executes the function of the other, the other executes the function of the former.

3. The semiconductor memory device according to claim 1, wherein

each of said bit lines and each of said virtual ground lines respectively have functions of the both and when one of them executes the function of the other, the other executes the function of the former.

4. The semiconductor memory device according to claim 1, wherein

the number of columns of said memory cells constituting said subarrays is 4.

5. The semiconductor memory device according to claim 1, wherein

said bit lines are connected to a common global bit line through a first selection transistor and said virtual ground lines are connected to a common global virtual ground line through a second selection transistor for each of said subarrays.

6. The semiconductor memory device according to claim 1, wherein a charging circuit is included which supplies a predetermined charging voltage to some or all of said bit lines and virtual ground lines of said subarrays in order to execute the reading operation.

7. The semiconductor memory device according to claim 6, wherein

said bit lines are connected to a common global bit line through a first selection transistor and said virtual ground lines are connected to a common global virtual ground line through a second selection transistor, and

said charging circuit charges said bit lines and said virtual ground lines to be charged through said global bit line and said global virtual ground line.

8. The semiconductor memory device according to claim 7, wherein in said subarrays including said memory cells from which data will be read,

at least one of said bit lines and one of said virtual ground lines to be connected only to said memory cells from which data will not be read are included as one of said bit lines and one of said virtual ground lines to be charged correspondingly to positions of said memory cells from which data will be read in said subarrays, and

said charging circuit charges said bit lines and said virtual ground lines to be charged at the time of the reading operation.

9. The semiconductor memory device according to claim 7, wherein in said subarrays including said memory cells from which data will be read,

at least one of said bit lines and one of said virtual ground lines to be connected only to said memory cells from which data will not be read are included as one of said bit lines and one of said virtual ground lines to be charged correspondingly to positions of said memory cells from which data will be read in said subarrays, and

said charging circuit charges said bit lines and said virtual ground lines to be charged during a charging period following the reading operation.

10. The semiconductor memory device according to claim 1, wherein

a switching transistor is set between said bit lines and said virtual ground lines adjacent to each other in said subarrays.

11. The semiconductor memory device according to claim 10, wherein

the number of columns of said memory cells constituting said subarrays is 4 and two out of four of said switching transistors set to each of said subarrays are controlled in common and two other switching transistors are controlled independently.

12. The semiconductor memory device according to claim 10, wherein in said subarrays including said memory cells from which data will be read,

said switching transistors set between said bit lines and said virtual ground lines to be connected to said memory cells from which data will be read are turned off at the time of the reading operation.

13. The semiconductor memory device according to claim 10, wherein

in said subarrays including said memory cells from which data will be read, said switching transistors set between said bit lines and said virtual ground lines to be connected to said memory cells from

which data will be read are turned off during a charging period following the reading operation.

14. The semiconductor memory device according to claim 1, wherein

said bit lines are connected to a common global bit line through a first selection transistor and said virtual ground lines are connected to a common global virtual ground line through a second selection transistor, and

a grounding switch transistor to be electrically connected with a ground line is set to said global bit line and said global virtual ground line respectively.

15. The semiconductor memory device according to claim 1, wherein

said bit lines are connected to a common global bit line through a first selection transistor and said virtual ground lines are connected to a common global virtual ground line through a second selection transistor for each of said subarrays, and

two of said first selection transistor or two of said second selection transistor to be connected to said bit line or said virtual ground line adjacent to each other at the both sides of boundaries between said subarrays are respectively controlled by a common control signal.

16. The semiconductor memory device according to claim 1, wherein

said memory cells are respectively constituted by a flash memory device or variable resistance device.

17. The semiconductor memory device according to claim 1, wherein

said memory cells respectively have a MOSFET structure and are respectively constituted by a sidewall memory device having a memory functional body on the sidewall of at least either of the drain side and source side for a gate.

18. The semiconductor memory device according to claim 17, wherein

a circuit for supplying programming voltages different from each other and said memory cell array are constituted so that the voltages can be applied to said bit lines and said virtual ground lines to be connected to said memory cells in which data will be programmed for programming operations of said memory cells in said subarrays.

19. The semiconductor memory device according to claim 18, wherein said sidewall memory device;

has a memory functional body at the both of the drain side and source side to a gate,

controls voltages to be applied to said bit lines and said virtual ground lines to be connected to said selected memory cells in accordance with a memory-functional-body selection signal for selecting either of said memory functional bodies in said memory cells, and

applies the programming operation or reading operation to said two memory functional bodies respectively by changing current directions for said selected memory cells in accordance with said voltage control.

20. The semiconductor memory device according to claim 19, wherein

said memory-functional-body selection signal serves as a part of an address signal.

21. The semiconductor memory device according to claim 19, wherein by selecting one of said memory cells and changing said memory-functional-body selection signal,

a voltage to be applied to said bit lines and said virtual ground lines to be connected to said selected memory cells is reversed before and after the change of said memory-functional-body selection signal to continuously apply the programming operation or reading operation to said two memory functional bodies of said selected memory cells.